AMENDMENTS IN THE CLAIMS

1. (currently amended) In a data processing system having a coherent memory hierarchy that includes a memory and a plurality of caches each assigned to particular ones of a plurality of devices that generate cache access operations, a method of maintaining cache coherency comprising:

when a first device ~~issuing~~ issues a particular [[an]] address operation, which operation requests[[ing]] sole ownership of a cache line and indicates that said first device intends to overwrite the cache line in a first cache[[;]], changing a coherency state of the cache line within said first cache to a first coherency state, which [[that]] indicates that the first device has sole ownership of the cache line ~~and~~ AND may or may not overwrite the cache line, wherein said particular address operation further causes a second device that has a most coherent copy of the cache line to not issue the most coherent copy of the cache line on the system bus;

in response to snooping said particular address operation, changing a coherency state of the cache line in a second cache associated with a snooping device to a second state without sending data from said cache line in the second cache to the first cache, wherein a default